REMARKS

Claims 1-6 and 8-30 remain pending in the present application. Claim 7 has been cancelled. Claim 23 and 25-27 have been amended to correct an inadvertent errors.

Objections to the Specification

The specification was objected to because the phrase "source store instruction" as recited in claims 1-7 and 28-30 is not specifically recited in the specification. Paragraph 0030 has been amended to insert the phrase and others as appropriate from the content of the application as filed.

Claim Objections

Claim 7 was objected to as being a method claim dependent on a claim to a processor. This claim has been cancelled making the objection moot.

Claim Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 1-7, 15-17, 23 and 25-30 were rejected under 35 U.S.C. § 112, second paragraph as failing to distinctly claim the present invention. In particular, the Office Action objects to the terms "source store instruction" and "source store address" that appear in several of these claims. Paragraph 0030 has been amended to insert these phrases as appropriate from the content of the application as filed. Claim 23 was rejected because of its dependency on claim 22. Claim 23 has been amended to correct this error and now depends from claim 21. In view of the amendments

to the specification and claims, reconsideration and withdrawal of the rejection of claims 1-7, 15-17, 23 and 25-30 under 35 U.S.C. § 112, second paragraph is respectfully requested.

Claim Rejections under 35 U.S.C. § 102

Claims 1-2, 4-5, 7-11, 13-16, 18-21, 23-26, and 28-29 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,751,983 to Abramson et al. ("Abramson"). Claims 3, 6, 12, 17, 22, 27, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Abramson.

In processor technology, when a load is predicted to be memory renamed to a previous store the prediction needs to be checked, that is, the memory renamed load is disambiguated, to determine whether the store is still in a memory ordering buffer ("MOB") when the memory renamed load retires. Since the memory renaming prediction occurs in the front-end of the processor, data consumption occurs early in the execution pipeline and the memory renamed load is not checked against the stores in the processor until the end of the execution pipeline, it is possible that the store to which the memory renamed load was predicted to forward from may have been de-allocated from the MOB. As stated in the specification, if the store has been deallocated, checking cannot be done and the memory renamed load must re-execute even if it was correct. Re-execution of the load instruction negatively impacts processor performance.

Embodiments of the present invention may be used when the store to which the memory renamed load was predicted to forward from has been de-allocated from the MOB. In accordance with an embodiment of the present invention, a trailing store buffer (TSB) may be used to maintain information from the stores that have been de-allocated from the MOB when the memory renamed load disambiguates. A generation number or color may be associated with the store information so that the memory renamed loads do not hit on younger allocated stores

(that is, stores that executed subsequent to the memory renamed load). In accordance with embodiments of the present invention, the TSB may store information for all stores that are de-allocated from the MOB or only for those stores that have memory renamed loads associated with them.

Independent claim 1 refers to a MOB to maintain a source store instruction and a TSB to maintain an address for said source store instruction, if said source store instruction has been de-allocated from the MOB.

Abramson does not discuss de-allocation of the MOB or any other structure in its patent. The text of Abramson cited in the Office Action is reproduced below:

> In one implementation, PAB 600 receives and saves the 24 highest order bits of the translated physical address for STORE and LOAD operations. In cooperation with the MOB 503 and MIU 304, these addresses are executed at the appropriate time. Tag array 601 stores the physical address tags of the data currently being cached in data array 602 and tag matches the accessing physical addresses against the stored physical address tags. Data array 602 receives and stores the data currently being cached and responds to data LOADs. In the embodiment of FIG. 5, tag array 601 and data array 602 store 128 sets of 2-way set associative 32-byte cache lines of data and their corresponding address tags.

Though a data array 602 is provided to store an output of the MOB, there is nothing in this section that teaches that the TSB is to maintain an address for a store instruction if that instruction has been de-allocated from the MOB.

In the rejection of claim 8 (and claims 18 and 28), the Office Action states that "entries received from the MOB are de-allocated at the MOB and are written to the data array." (pg. 6), but nothing in this cited section supports this conclusion. The data array 602 is part of the data cache 205, which is responsible for fetching data for a physical address associated with a LOAD instruction and storing data to a physical address associated with a STORE instruction.

Since features of the claims are neither taught nor suggested by Abramson. Reconsideration and withdrawal of the rejection of claims 1-6 and 8-30 under 35 U.S.C. §§ 102(b) and 103(a) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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